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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,861	08/09/2004	Anindya SAHA	TI-36220	4860

23494 7590 10/03/2007

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EXAMINER
ALMO, KHAREEM E

ART UNIT	PAPER NUMBER
2816	

NOTIFICATION DATE	DELIVERY MODE
10/03/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/710,861	SAHA ET AL.	
	Examiner	Art Unit	
	Khareem E. Almo	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/14/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17 and 20-28* is/are rejected.

7)☒ Claim(s) *18,19,29 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/14/2005*, 8/20/2004
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4 and 12-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Carobolante (US 6211727).

With respect to claim 1, Figure 2 of Carbolante discloses a method (via the device in Figure 2) of providing optimal supply voltage to an integrated circuit, said method comprising: providing a supply voltage (Vsup) to said integrated circuit; measuring (via 22) a characteristic at a plurality of portions on said integrated circuit to generate corresponding measured values (output at VPRFM); and adjusting said supply voltage (via 16, 32 and 28)to an optimum value based on said measured values. (See also claim 34, column 10 lines 16-32).

With respect to claim 2, Figure 2 of Carbolante discloses a method (via the device in Figure 2) of claim 1, wherein said characteristic comprises a propagation delay (propagation delay of individual devices of 22) of signals in each of said plurality of portions (22).

With respect to claim 3, Figure 2 of Carbolante discloses a method(via the device in Figure 2) of claim 2, wherein a high measured value of said propagation delay indicates a weak process corner on said integrated circuit, and a low measured value

indicates a strong process corner on said integrated circuit.

With respect to claim 4, Figure 2 of Carbolante discloses a method(via the device in Figure 2) of claim 3, wherein said adjusting comprises increasing said supply voltage (via 32 and 16) if said propagation delay (determined by devices 22) has said high measured value (depending on how Vref is set) and decreasing said supply voltage (via 32 and 16) if said propagation delay has said low measured value (depending on how Vref is set).

With respect to claim 12, Figure 2 of Carbolante discloses a device comprising: an application block (12) implementing a user application; a power management block (18) providing a supply voltage (Vsup) to said application block; a measurement block (14) measuring a characteristic at a plurality of portions on said application block to generate corresponding measured values(at the outputs of each 22); and a processing unit (16) interfacing with said power management block to adjust said supply voltage to an optimum value based on said measured values (outputs of 22).

With respect to claim 13, Figure 2 of Carbolante discloses device of claim 12, wherein said application block (12), said measurement block (14), said power management block (18) and said processing unit (16) are fabricated on a single die. (See column 3, lines 64-66 and column 4, lines 1-4).

With respect to claim 14, Figure 2 of Carbolante discloses the device of claim 13, wherein said characteristic comprises a propagation delay (between 22s inside 14) of a corresponding signal in said plurality of portions (22).

With respect to claim 15, Figure 2 of Carbolante discloses device of claim 14, wherein said measurement block (14) comprises a monitor block (first four 22s) generating said measured values representing said propagation delay at said plurality of portions, wherein said processing unit (16) determines a strength of process corner of said application block based on said measured values, and said power management block (18) adjusts said supply voltage (via 32) to an optimum value based on said strength.

With respect to claim 16, Figure 2 of Carbolante discloses device of claim 15, wherein said measurement block (14) further comprises a plurality of gated ring oscillators (GROs) (the first 4, 22s form a ring oscillator gated by the last 22), wherein each of said plurality of GROs is located at a corresponding one of said plurality of portions (22), said plurality of GROs generating a corresponding number of signals. (Note: with reference to the limitation of plurality of gated ring oscillators, because mere duplication of parts is not deemed to be patentable this limitation is not given patentable weight.)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 17, 20-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carbolante (US 6211727) in view of Lesea et al. (US 7088172)

With respect to claim 5, Figure 2 of Carbolante the method of claim 4, (via the device in Figure 2) of claim 3, wherein said adjusting comprises increasing said supply voltage (via 32 and 16) if said propagation delay (determined by devices 22) has said high measured value (depending on how Vref is set) and decreasing said supply voltage (via 32 and 16) if said propagation delay has said low measured value (depending on how Vref is set) but fails to disclose wherein the method further comprises receiving said measured values on a multiplexer and processing each of said measured values using a shared circuit. Figure 6 and 7 of Lesea et al. (US 7088172) teaches a configurable voltage bias circuit having a voltage divider that is able to compensate for temperature variations. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to substitute the frequency divider of Carbolante, with the frequency divider/ voltage bias circuit of Lesea et al. for the purpose compensating the temperature variations in the propagation delay output. The combination of the voltage divider (voltage bias circuit) of Lesea et al. as the frequency divider (24) of Carbolante would produce the claim limitation wherein the method further comprises receiving said measured values on a multiplexer (710) and processing (via 26) each of said measured values using a shared circuit.

With respect to claim 6, the combination above produces the method of claim 5, wherein said adjusting comprises: selecting a maximum value and a minimum value (via 710) from said measured values; and determining whether to increase or decrease (via 26) said supply voltage (Vsup) based on said maximum value.

With respect to claim 7, the combination above produces the method of claim 6,

wherein said adjusting further comprising: checking whether a ratio of said maximum value and said minimum value exceeds a pre-specified threshold (input at Vref); and using a next highest value instead of said maximum value in said determining.

With respect to claim 8, the combination above produces the method of claim 6, further comprising: determining a first value, a second value and a third value corresponding to a weak process corner, a nominal process corner and a strong process corner respectively for a present supply voltage (Vsup); and discarding said integrated circuit as being unusable if said maximum value (at (+) terminal) is more than a first multiplier (input at Vref) of said first value or if said maximum value (at (+) terminal) is less than a second multiplier (input at Vref) of said third value.

With respect to claim 6, the combination above produces the method of claim 6, wherein said determining determines to increase (via 32) said supply voltage (Vsup) if said maximum value is less than a first multiplier (input at Vref) of said first value and if said maximum value is more than a second multiplier (input at Vref) of said third value.

With respect to claim 10, the combination above produces the method of claim 6, wherein said determining determines to decrease (via 32) said supply voltage (Vsup) if said maximum value is less than a first multiplier (input at Vref) of said third value and if said maximum value is more than a second multiplier (input at Vref) of said third value.

With respect to claim 11, the combination above produces the method 11. The method of claim 1, further comprises programming a register (control register

720 of Leasa et a) with an adjustment value, wherein said adjustment value represents said optimum value of said supply voltage (Vsup), wherein said adjusting uses said adjustment value to adjust said supply voltage (Vsup) while initializing said integrated circuit.

5. Claims 17, 20-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carbolante (US 6211727) in view of Lesea et al. (US 7088172)

With respect to claim 17, Figure 2 of Carbolante the device of claim 14, wherein said measurement block (14 and 24) comprises a monitor block (14 and 24) generating said measured values representing said propagation delay at said plurality of portions, wherein said processing unit (26) determines a strength of process corner of said application block based on said measured values, and said power management block (18) adjusts said supply voltage (via 32) to an optimum value based on said strength, wherein said measurement block (14 and 24) further comprises a plurality of gated ring oscillators (GROs) (the first 4, 22s form a ring oscillator gated by the last 22), wherein each of said plurality of GROs is located at a corresponding one of said plurality of portions (22), said plurality of GROs generating a corresponding number of signals. (Note: With reference to the limitation of plurality of gated ring oscillators, because mere duplication of parts is not deemed to be patentable this limitation is not given patentable weight.), but fails to disclose the details of the frequency divider within the monitor block wherein said monitor block comprises a multiplexer to select one of said signals. Figure 6 and 7 of Lesea et al. (US 7088172) teaches a configurable

voltage bias circuit having a voltage divider that is able to compensate for temperature variations. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to substitute the frequency divider of Carbolante, with the frequency divider/ voltage bias circuit of Lesea et al. for the purpose compensating the temperature variations in the propagation delay output. The combination of the voltage divider (voltage bias circuit) of Lesea et al. as the frequency divider (24) of Carbolante would produce the claim limitation wherein said monitior block comprises a multiplexer (710) to select one of said signals.

With respect to claim 20, the combination above produces the device of claim 17, wherein a high value of said measured values indicates a weak process corner at a corresponding portion, and a low value of said measured values indicates a strong process corner at a corresponding portion.

With respect to claim 21, the combination above disclose the device of claim 20, wherein said processing unit (23) is operable to select a maximum value and a minimum value from said measured values (at input of (+) terminal based on Vref); and determine whether to increase or decrease said supply voltage based on said maximum value, wherein said power management block (18) increases (via 32) said supply voltage (Vsup) if said maximum value has said high value and decreases (via 32) said supply voltage (Vsup) if said maximum value has said low value.

With respect to claim 22, the combination above produces the device of claim 21, wherein said processing unit (26) is further operable to: check whether a ratio of said maximum value and said minimum value exceeds a pre-specified threshold (Vref);

and use a next highest value instead of said maximum value to perform said determine if said ratio exceeds said pre-specified threshold.

With respect to claim3, the combination above produces the device of claim 21, wherein said processing unit (26) is further operable to:receive a first value (at (-) terminal), a second value (at (-) terminal) and a third value (at (-) terminal) corresponding to a weak process a corner, a nominal process corner and a strong process corner respectively for a present supply voltage; and discard said single die as being unusable if said maximum value is more than a first multiplier of said first value (input at (+) terminal) or if said maximum value is less than a second multiplier (input at (+) terminal) of said third value.

With respect to claim 24, the combination above produces the device of claim 21, wherein said processing unit (26) determines to increase (based on Vref) said supply voltage (Vsup) if said maximum value is less than a first multiplier (input at Vref) of said first value and if said maximum value is more than a second multiplier (Input at Vref) of said third value.

With respect to claim 25, the combination above produces the device of claim 21, wherein said processing unit (26) determines to decrease (based on Vref) said supply voltage (Vsup) if said maximum value is less than a first multiplier (input at Vref) of said third value and if said maximum value is more than a second multiplier (input at Vref) of said third value.

With respect to claim 26, the combination above produces the device of claim 25, but fails to produce wherein the device further comprises a random access memory

(RAM) storing a lookup table containing measured values corresponding to a weak process corner, a nominal process corner and a strong process corner for a plurality of pre-determined levels of said supply voltage and said RAM provides said first value, said second value and said third value. It would be obvious to one skilled in the art at the time the invention was made to use a RAM as the served device of Figure 2 of Leasa for the purpose of controlling the voltage of applications to reduce power used by the RAM applications.

With respect to claim 27, the combination above is capable of producing the device of claim 26, wherein said maximum value comprises the largest value among said plurality of measured values and said minimum value comprises the smallest value among said plurality of measured values.

With respect to claim 28, the combination above produces the device of claim 15, wherein said power management block(18 of Carbolante and 720 of figure 7 of Lesea et al.) comprises: a register (720) programmed to store an adjustment value, wherein said adjustment value causes said power management block to provide said optimum value of said supply voltage (Vsup) while initializing said single die.

Allowable Subject Matter

6. Claims 18-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claim 18, the prior art of record fails to suggest or disclose a a counter receiving a clock signal and counting a number of clock periods of said clock signal between two successive transitions generated by said transition detector to generate a measured value corresponding to said output, wherein said measured value is comprised in said plurality of measured values as disclosed

With respect to claim 19, the prior art of record fails to disclose a counter generating a measured value by counting number of cycles in an output generated by said multiplexer during a fixed time period, wherein said measured value is comprised in said plurality of measured values.

With respect to claim 29 and 30, the prior art of record fails to suggest or disclose a second multiplexer selecting one of said adjustment value or an output value of said processing unit as a multiplexer output.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khareem E. Almo whose telephone number is (571) 272-5524. The examiner can normally be reached on Mon-Fri (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on (571) 272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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